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| EXAMINER |
|---|
| DOAN, DUC T |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | Application No. | Applicant(s) |
| **Office Action Summary** | 10/815,294 | BARRY ET AL. |
| | Examiner | Art Unit | |
| | Duc T. Doan | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>30 July 2004</u>.

2a)☐ This action is **FINAL**.      2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

# DETAILED ACTION

## *Status of Claims*

Claims 1-19 are in the application.

Claims 1-19 are rejected.

## *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless -

(a) the invention was known or used by other's in this country or patented or described in a printed

publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public

use or on sale in this country, more than one year prior to the date of application for patent in the United

States.

(e) the invention was described in a patent granted on an application for patent by another fled in the United

States before the invention thereof by the applicant for patent, or on an international application by another

who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the

invention thereof by the applicant for patent.

Claim 1 is rejected under 35 U.S.C. 102 (b) as being anticipated by Saulsbury et al (US

2002/0032710).

As in claim 1, Saulsbury describes a processor address translation apparatus for translating an instruction operand address to a different operand address (Saulsbury's Fig 6A, paragraph 20), the processor address translation apparatus comprising: a memory with an address input for selecting a data element from a plurality of data elements (Saulsbury's Fig 1: #32-1 dram); an instruction register for receiving an instruction encoded with an operand address and control information indicating the operand address is to be translated as part of the instruction's execution (Saulsbury's paragraphs 44,46 VLIW instructions load store; VLIW sub-instructions Fig 4) ; and an address translation unit for accessing the memory in a translation pattern, having the operand address as input and, in response to the instruction received in the instruction register, translating the operand address to form the different operand address in accordance with the translation pattern (Saulsbury's Fig 5 shows instructions translating operands rw,rx,ry,rz) , the different operand address accessing a data element from the memory through the address input (Saulsbury's paragraphs 24-25,35 describe distributed shared memory accessible by processor's load store commands, the memory accessed by operand addresses of instruction as described in paragraph 44,lines 10-13).

## *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the

manner in which the invention was made.


Claims 2 ... rejected under 35 U.S.C. 103(a) as being unpatentable over Saulsbury

et al (US 2002/0032710).

As in claim 2, Saulsbury describes wherein the address translation unit further comprises:

a plurality of translation parameters and address translation functions supporting

a plurality of translation patterns; and an input to select a translation pattern from the plurality of

supported translation patterns. Saulsbury's page 6 paragraph 67 describes VLIW is configured to

operate with multiple patterns of matrix transpose; Thus obviously, an input to the address

translation circuits is required to indicate/select one of these different patterns for the processor

and address translation circuits to operate on one of these patterns.


Claims 3-10,16-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Saulsbury

et al (US 2002/0032710) as applied to claim 2 and in view of Nair et al (US 6944747).

As in claim 3, the claim recites the processor address translation apparatus of claim 2

wherein the translation parameters include k by k s bits and k e bits for a k bit address and

address translation functions further comprises combinatorial logic governed by the following

equations; The claim further recites an equation to process matrix transpose of operand

addresses. The claim's matrix transpose includes a function (e bits) to provide bit-wise invert of

input operand address besides and, xor functions. Saulsbury does not describe the claim's detail

of the matrix transpose. However, Nair describes an apparatus for matrix processing that can

manipulate addresses bits using matrix multiply, addition, subtraction, bit-reverse operations

etc..Nair teaches for these matrix operations, it is required the matrix transpose to have functions

of bit-wises shifting, logical and, or, xor and bit inverting (i.e NOR, NAND) etc...(Nair's

column 12, table 1) Thus it is obviously, the transpose matrix must includes the claim's e-bits

vector since this vector merely providing the bit-wise invert function in the matrix transpose. It

would have been obvious to one of ordinary skill in the art at the time of invention to include the

matrix transposes as suggested by Nair in Saulsbury's system by storing the predetermined

matrix transposes in a memory that is permanently or dynamically loaded into the system when

needed; thereby providing the capability to quickly perform matrix operations.

As in claim 4, the processor address translation apparatus of claim 1 wherein the

processor instruction is a block load instruction (Saulsbury's paragraph 66 describes the matrix

operates on 16 elements in a 4 by 4 matrix).

As in claim 5, the claim recites the processor address translation apparatus of claim 1

disposed within a plurality of instruction operand address paths for a plurality of instructions, the

plurality of instructions fetched for simultaneous execution (Saulsbury's paragraph 33 describes

the VLIW sub-instructions are distributed to corresponding processing paths Fig 2: #56).

As in claim 6, Saulsbury describes wherein the plurality of instructions constitutes a very

long instruction word VLIW (Saulsbury's paragraph 33).

As in claim 7, the rationale in the rejection of claims 1 and 2 is incorporated herein.The

claim recites a processor register file indexing (RFM address translation apparatus for translating

an RFI sequence of instruction operand addresses to an RFI sequence of different operand

addresses, the processor RFI address translation apparatus comprising:

a memory with an address input for selecting a data element from a plurality of data

elements (Saulsbury's Fig 1: #32-1)

an instruction register for receiving an instruction encoded with an operand address and

control information indicating the operand address is to be translated as part of the instruction's

execution (Saulsbury's Fig 3);

an RFI update unit enabled to generate on the RFI update unit's output a linear

sequence of RFI operand addresses in response to a received sequence of RFI translation

type instructions (Saulsbury's paragraph 45,52 describes circuits required for decoding various

instruction types, generates a sequence of source operands addresses for an VLIW sub-

instruction; the destination operand addresses are used to update the register file for the next

operation. The operation in block of matrix further requires a linear sequence of source and

destination operand addresses specified in the sub-instructions).

A multiplexer for selecting between the operand addresses from the instruction

Register for a first RFI operation and selecting the RWI update unit's output for subsequent

RFI operations. (Salisbury's paragraphs 45,46 clearly describe the destination operand

address/destination register of the current instructions are multiplexed and feedback to the source

operand/source register for the subsequence instruction).

An address translation unit for accessing the memory in a translation pattern, receiving a

sequence of operand addresses from the multiplexer and, in response to the sequence of RFI

operand addresses, translating the sequence of RFI operand addresses to form a sequence of

different operand addresses in accordance with the translation pattern, the different operand

addresses each accessing a data element from the memory through the address input (Salisbury's

paragraphs 51,52 describes the circuits for a matrix transpose operation on a block of operand

addresses).

As in claim 8, the claim recites the processor RFI address translation apparatus of claim 7

disposed within PEs of an array of PEs. (Saulsbury's Fig 2, paragraph 34 describes circuits to

process sub-instructions are correspond directly to each processing paths, Fig 2: #56. Thus each

processing path that corresponds to the claim's PE contains address translation circuit for it's

own register file, Fig 2: #60-1, #60-2).

As in claim 9, Saulsbury describes he processor RFI address translation apparatus of

claim 7 disposed within a plurality of instruction operand address paths for a plurality of

instructions, the plurality of instructions fetched for simultaneous execution. Saulsbury's

paragraphs 34 describes using multiple processing paths that process instructions in a parallel

manner help improve performance of the processing core.

Claim 10 rejected based on the same rationale as in the rejection of claim 6.

Claim 16 rejected based on the same rationale as in the rejection of claim 4.

Claim 17 rejected based on the same rationale as in the rejection of claim 3. It's

obviously that  matrix transpose operations AND,OR,XOR etc. as described by Nair must use

combination logic.

Claim 18 rejected based on the same rationale as in the rejection of claims 1,3.

Claim 19 rejected based on the same rationale as in the rejection of claim 3.

Claims 11-15 rejected under 35 U.S.C. 103(a) as being unpatentable over Saulsbury et al

(US 2002/0032710), in view of Nair et al (US 6944747) and further in view of Dowling (US

6823505)

As in claim 11, the claim recites an address translation memory device for accessing data

at translated addresses, the address translation memory device comprising: a first read address

input (Dowling's Fig 2: #114 address register pointer), a storage device having data accessible at

addressable locations (Dowling's register array, Fig 2: #102; Fig 6: register array A, B), a

second read address input for selecting data from the storage device during read operations, and a

data output port (Dowling's Fig 2: #120 corresponding data memory of the register array); and

an address translation unit for accessing the storage device in a translation pattern (Dowling's

Fig 3C, address translation pattern), the address translation unit translating the first read address

input in accordance with the translation pattern, to the storage device second read address input

for reading data from the storage device at a translated address during a read operation

(Dowling's Fig 2: #203, translated address is selected to address the register array, for example

in read operation). The claim rejected based on the same rationale as in the rejection of claims 1

and 2

. Saulsbuy does not explicitly describe the claim's detail circuit components of the address

translation memory device. However, Dowling describes multiple address translation unit,

(Dowling's Fig 2: #212) in functional units that share register array such as register file A,

register file B shown in Fig 6. It would have been obvious to one of ordinary skill in the art at the

time of invention to include multiple address translation units (Dowling's Fig 2: #212, Fig 6) as

taught by Dowling in Saulsbury's system to share addresses in register files thereby allowing

multiple operations executed concurrently using shared address values in register files (Dowling's column 15, line 49 to column 16 line 14).

As in claim 12, the claim rejected based on the same rationale as in the rejection of claim 11. Dowling's Fig 6 clearly shows multiple address translation units operates in both read and write operations.

As in claim 13, the claim recites wherein the storage device further comprises location selection logic merged with the address translation unit. Dowling's Fig 2,Fig 3A show the address translation unit #212 includes selection logic for registers in the register file array.

Claim 14 rejected based on the same rationale as in the rejection of claim 2.

Claim 15 rejected based on the same rationale as in the rejection of claim 3.

### *Conclusion*

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
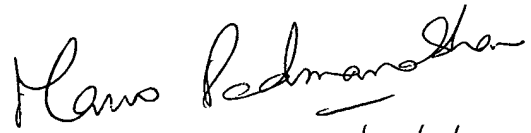
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DD.

Mano Padmanabhan

Supervisory Patent Examiner

TC2188

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SUPERVISORY PATENT EXAMINER